REMARKS

This response is to the Office Letter mailed in the above-referenced case on March 04, 2003. Claims 1-32 are presented for examination. In the Office Letter the Examiner has rejected claims 1-32 under 35 U.S.C. 102(e) as being anticipated by Chang (U.S. 5,634,015), hereinafter Chang. The Examiner points out that the claims are numbered incorrectly.

In response to the Examiner's rejections and comments, applicant herein provides arguments to more particularly point out the subject matter regarded as inventive by applicant and unarguably distinguish applicant's invention over the art of Chang presented by the Examiner. The numbering of the claims is herein corrected by amendment.

Regarding claims 1, the Examiner states Chang teaches Background Event Buffer Manager (Generic Adapter Manager 18), a data processing system (Generic High Bandwidth Adapter Col. 9, Ln 45-49), Events ("packets... Col. 1- Ln 33-67), a processor (processor subsystem (P) 14 Col. 9 Ln 50-67), a port (adapter port), a queuing function (PMI 20, Col. 10 Ln 40-67, GAM primitives Col. 14, Ln 1-19), a Notification Function (GAM Col. 11 Ln 33-37), and characterized in that the BEBM handles all event ordering and accounting for the processor (GAM 18 Col. 10 Ln 42-44, Col 11 Ln 22-25, "packet enqueue/dequeue..."Col. 14 Ln 1-4).

Applicant respectfully traverses the Examiner's above interpretation of Chang. Applicant's claim 1 clearly recites that the BEBM handles **all** event ordering and accounting for the processor. Applicant argues that the GAM 18 of Chang fails to read on the claimed functions of applicant's BEBM.

The Examiner states that the GAM 18 of Chang consists of a port (adapter port). Applicant's claim 1 recites that the BEBM comprises a port for receiving event identifications (IDs) from a device. Applicant argues that the

GAM 18 of Chang does not receive event ID's from an originating device. The adapter port referred to by the Examiner could only be understood by applicant as the PMI 20. Applicant points out that Col. 14 beginning at line 1-41 describes GAM 18 primitives and response, Gam 18 local operations, and P14 Direct Control Messaging. Lines 1-4 of Col. 14 teach that Gam primitives are invoked whenever the P or a PMI requires the GAM to perform packet memory management functions such as packet enqueue/dequeue or free buffer allocations. Lines 30-41 of Col. 14 recites that the adapter architecture allows the P to access the GAM local memory in order to provide extensive diagnostic capability and future GAM function enhancement. Further the referenced portion of Chang teaches that the P direct control message is used by the P to control and program the PMI and the adapter port internal hardware. Lines 64-66 of Chang's column 14 teaches that when a packet is received by an adapter port, the PMI will store the packet data along with the packet header control information into the PM.

Applicant argues that not only does the GAM 18 of Chang not have a receiving port as claimed, but also fails to handle all event ordering and accounting for the processor as claimed in applicant's invention. As clearly taught in column 14 of Chang the processor P controls and programs the IPM 20, adapter ports, and must instruct the GAM itself. Therefore, the processor (P) of Chang must still handle much of the accounting and ordering performed by the BEBM of applicant's invention.

Further, applicant points out that Chang teaches when the P or PMI 20 needs buffer space to receive a packet, it makes a buffer request to the GAM 18. Packets are further organized into queues 36. Each PMI in the adapter has several queues assigned to it for input and output. After a packet is moved into the PM the PMI will command the Gam to place the packet into a particular queue. Eventually, Chang teaches, the Gam will notify the P that packets are ready for processing. Code running on the P will dequeue the packets, process

them, and then enqueue them into output queues. Applicant argues that Chang's P, or the PMI, which is controlled by the P, is doing much of the queuing, ordering and accounting of packets to be processed.

Applicant's specification points out that the amount of time the processor dedicates to these kinds of tasks can be significant, thus diminishing the performance of the processor on the processing of the events. Moreover, depending on how frequent these events occur, and the amount of processing that each event takes, the processor will not be able to start processing them at the

time they occur. Therefore, the processor will need to buffer the events and process them later on.

Clearly, the ordering of and accounting for events, as described herein, is a considerable and significant processor load. The BEBM of applicant's invention performs all of the event ID ordering and accounting, leaving the processor free to only process packets.

Offering the arguments above, applicant believes the present invention easily distinguishes over the art of Chang. Therefore, claim 1 is patentable over the art of Chang. Claims 2-8 are patentable on their own merits, or at least as depended from a patentable claim.

Independent claims 9, 17 and 25 are rejected by the Examiner using the same or similar reasoning provided on behalf of claim 1. Therefore, applicant believes these claims are also patentable in view of the arguments provided by applicant on behalf of claim 1. Claims 10-16, 18-24, and 26-32 are patentable on their own merits, or at least as depended from a patentable claim.

As all of the claims have been shown to be patentable over Chang, applicant respectfully requests that this application be reconsidered, the claims be allowed, and that this case be passed quickly to issue.

If there are any time extensions needed beyond any extension specifically requested with this amendment, such extension of time is hereby requested. If

there are any fees due beyond any fees paid with this amendment, authorization is given to deduct such fees from deposit account 50-0534.

Respectfully Submitted,
Mario Nemirovsky et al.

by _____
Donald R. Boys
Reg. No. 35,074

Donald R. Boys
Central Coast Patent Agency
P.O. Box 187
Aromas, CA 95004
(831) 726-1457